IN THE SPECIFICATION

Please amend paragraph 0022 of the specification as follows:

[0022] In FIG. 4, a virtual register map 112 has 128 virtual registers VR(0)-VR(127) used to map frames of data to register file 114, with 160 registers GR(0)-GR(159), the stacked registers being GR(M+1)-GR(Q) = GR(32)-GR(159). Specifically, virtual registers VR(0)-VR(31) map one-to-one with static registers GR(0)-GR(31), between mapping lines 140, 142. Virtual registers VR(32)-VR(127) map to frames of physical registers starting anywhere GR(32)-GR(159) between mapping lines 144, 146. At the same time, hazard detect through register ID file 115 aliases physical registers GR(32)-GR(159) in hazard detect capability. More particularly, hazard detection logic 117 detects data hazards for multiple register IDs corresponding to multiple rows of register file 114; hazard detection is thus not unique for each row. If for example the register ID file has 32 register identifiers, then each subsequent set of 32 GRs beginning with GR(32) (e.g., GR(32:63), ~~GR(65:95).~~ GR(64:95), GR(96:127) and GR(128:159)) alias respectively to the same 32 hazard detect register identifiers RID(32:63), as illustrated in FIG. 4. Specifically, in this example, register IDs now alias to common hazard detect logic for rows GR(32), GR(64), GR(96), for rows GR(33), GR(65), GR(97), and so on, of register file 114. Mapping lines 148 illustrate that RID(0:31) maps to GR(0:31). RID(32:63) maps to each set GR(32:63), GR(64:95), GR(96:127), GR(128:159) illustratively by mapping lines 150.